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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/670,434	09/23/2003	Pinghai Hao	TI-35470	2415

23494 7590 07/26/2005

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EXAMINER	
NGUYEN, KHIEM D	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 07/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/670,434	HAO ET AL.	
	Examiner	Art Unit	
	Khiem D. Nguyen	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

New Grounds of Rejection

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Fisher (U.S. Patent 6,391,733).

In re claim 1, **Fisher** discloses a method for fabricating a transistor structure, comprising the steps of: providing a substrate **12** and forming a lightly doped drain (LDD) region **46, 48** in the substrate **12** (FIG. 4);

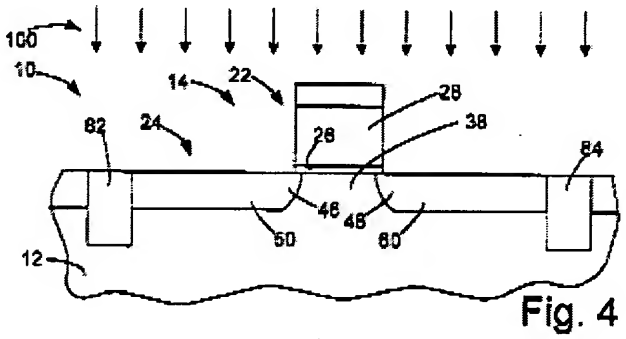

Fig. 4

implanting a first dopant **100** has a lower dopant concentration (10^{12}-10^{15} atoms/cm^2) than that of the associated **120** LDD region **46,48** (1x 10^{12}- 1x10^{16} atoms/cm^2) into the lightly doped drain (LDD) region **46, 48** to a depth less than a LDD junction depth (col. 4, line 45 to col. 5, line 34 and FIG. 7); and

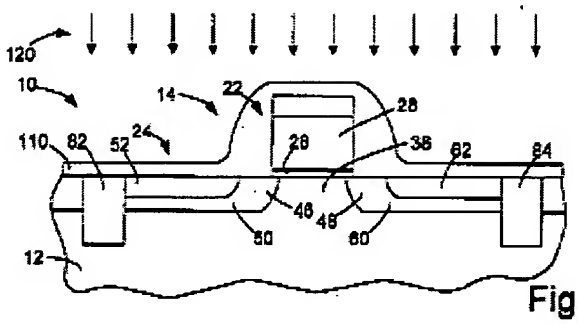

Fig. 7

implanting a second dopant **130** into the substrate **12** beyond the LDD junction depth to form a source/drain region **54,64,** the implantation of the second dopant overpowering ($5x10^{14}$-$1x10^{16}$) atoms/cm^2 a substantial portion of the first dopant to define a floating region **52, 62** of the first dopant within the LDD region 46, 48 (col. 5, lines 43-54 and FIG. 9).

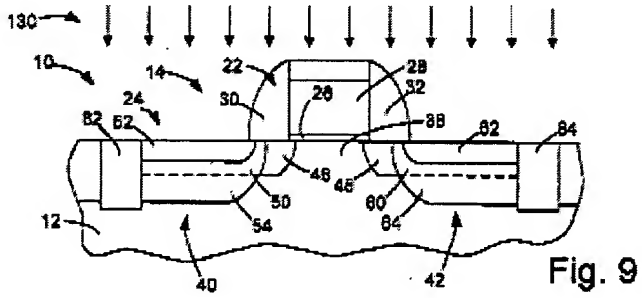

Fig. 9

In re claim 2, **Fisher** discloses that the floating region further comprising a floating ring **52, 62,** substantially self-aligned with an edge of a gate **28** of the transistor structure **14** (col. 5, lines 19-34 and FIG. 9).

In re claim 3, **Fisher** discloses that the method of claim 1, further comprising forming the LDD region **46, 48** by implanting a dose 120 ($1x10^{12}$-$1x10^{16}$ atoms/cm^2) of an LDD dopant that is greater than a dose of the first dopant 100 (10^{12}- 10^{15} atoms/cm^2) (col. 4, line 45 to col. 5, line 34 and FIGS. 4 and 7).

In re claim 4, **Fisher** discloses that the dose of the first dopant **100** being about twenty-percent or less of the dose of the LDD dopant **120** (col. 4, line 45 to col. 5, line 34 and FIGS. 4 and 7).

In re claim 5, it is well-known to one of ordinary skill in the art at the time of the invention was made that the at least one of the implantation of the first dopant and the implantation of the LDD dopant employing tilted angle implants to enhance an amount of overlap between a gate structure of the transistor structure and the LDD region.

In re claim 6, **Fisher** discloses that the dose of the second dopant **130** ($5x10^{14}$-$1x10^{16}$ atoms/cm^2) being greater than the dose of the LDD dopant **120** ($1x10^{12}$-$1x10^{16}$ atoms/cm^2) (col. 5, lines 19-54 and FIGS. 7 and 9).

In re claim 7, **Fisher** discloses that the implantation of the LDD dopant further comprising implanting a dose of n-type dopant in the range from about ($1x10^{12}$-$1x10^{16}$ atoms/cm^2), and the implantation of the first dopant **100** further comprising implanting a dose in a range from about (10^{12}-10^{15} atoms/cm^2) of a p-type dopant (col. 4, line 45 to col. 5, line 34).

In re claim 8, **Fisher** discloses that the transistor structure is a complimentary metal oxide semiconductor (CMOS) structure that includes a gate **28** having a side edge portion, the floating region **52, 62** being substantially aligned with the side edge portion of the gate **28** (FIG. 9).

In re claim 9, **Fisher** discloses that the CMOS structure is an n-channel CMOS structure, the first dopant **100** forming a shallow region in the LDD region that comprises a p-type dopant (FIG. 4).

In re claim 10, **Fisher** discloses that the first dopant **100** comprises boron (B), and the floating region **52, 62** further comprises a boron floating ring, substantially aligned with side edge portion of the gate **28** (col. 4, lines 45-53 and FIGS. 4 and 9).

In re claim 11, **Fisher** discloses that the CMOS structure is a p-channel CMOS structure, the first dopant **100** defining a shallow region that comprises an n-type dopant (FIGS. 4 and 9).

In re claim 12, **Fisher** discloses that the method of claim 1, further comprising: forming a gate structure **28** above the substrate **12**, the LDD region **46, 48** and the source/drain region **54, 64** being formed in the substrate **12** generally around the gate structure **28** the gate structure overlapping at least a substantial portion of the LDD region **46, 48** and the floating ring **52, 62** being substantially aligned with an edge of the gate structure 28 (FIG. 9).

In re claim 13, **Fisher** discloses a method for fabricating a CMOS transistor device, comprising the steps of forming a gate structure **28** on a substrate **12**, the gate structure **28** having a side edge;

forming a lightly doped drain (LDD) region **46, 48** in the substrate **12** laterally of a channel region **38** and extending beneath the gate structure (FIG. 4);

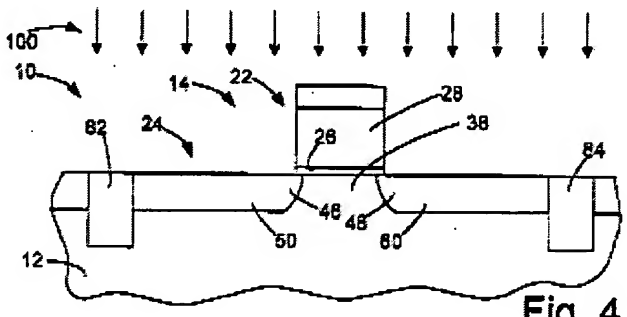

Fig. 4

then forming a shallow region (10^{12}-10^{15} atoms/cm^2) in the LDD region **46, 48** having a lower concentration than that of the associated LDD region ($1x10^{12}$-$1x10^{16}$ atoms/cm^2) that extends into the substrate **12** to a depth that is less than an LDD junction depth and spaced from the channel region (col. 4, line 45 to col. 5, line 34 and FIGS. 4 and 7); and

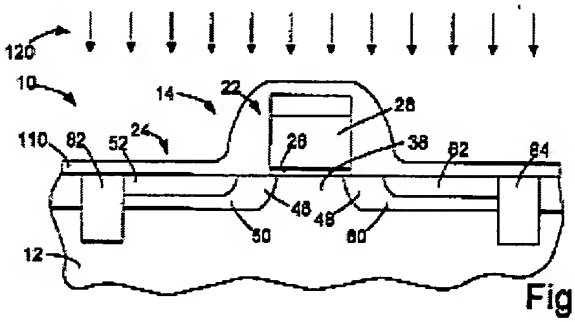

Fig. 7

forming a source/drain region **54,64**, the formation of the source/drain region resulting in forming a floating structure **52, 62** from the shallow region that is located in the LDD region **46, 48** and generally aligned with the side edge of the gate structure 28 (col. 5, lines 43-54 and FIG. 9).

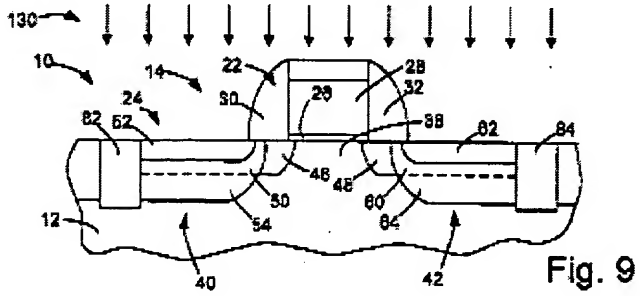

Fig. 9

In re claim 14, **Fisher** discloses that the LDD region **46, 48** being formed with a dose ($1x10^{12}$-$1x10^{16}$ atoms/cm^2) of a dopant that is greater than a dose of a dopant utilized

to form the shallow region (10^{12}-10^{15} atoms/cm^2) (col. 4, line 45 to col. 5, line 34 and FIGS. 4 and 7).

In re claim 15, **Fisher** discloses that the dose of the dopant **100** that is utilized to form the shallow region is at least approximately twenty-percent less than the dose of the dopant **120** that is utilized to form the LDD region **120** (col. 4, line 45 to col. 5, line 34 and FIGS. 4 and 7).

In re claim 16, **Fisher** discloses the formation of the LDD region **46, 48** further comprising implanting a dose **120** of n-type dopant in a range from about ($1x10^{12}$-$1x10^{16}$ atoms/cm^2), and the formation of the shallow region further comprising implanting a dose 100 in a range (10^{12}- 10^{15} atoms/cm^2) (col. 4, line 45 to col. 5, line 34 and FIGS. 4 and 7).

In re claim 17, it is well-known to one of ordinary skill in the art at the time of the invention was made that the at least one of the implantation of the formation of the LDD region and the formation of the shallow region further comprising employing tilted angle implants to increase an amount of overlap beneath the gate structure.

In re claim 18, **Fisher** discloses that the formation of the source/drain region **54, 64** being implemented with a dose of a dopant ($5x10^{14}$-$1x10^{16}$ atoms/cm^2) that is greater than a dose of a dopant utilized to form each of the LDD region **120** ($1x10^{12}$-$1x10^{16}$ atoms/cm^2) and the shallow region (col. 5, lines 19-54).

In re claim 19, **Fisher** discloses that the CMOS structure is an n-channel CMOS structure, the shallow region comprising a p-type dopant (col. 4, line 45 to col. 5, line 54).

In re claim 20, **Fisher** discloses that the shallow region comprising boron (B), the floating structure **52, 62** comprising a boron floating ring **52, 62** substantially aligned with the side edge of the gate structure **28** (col. 4, lines 45-53 and FIGS. 4 and 9).

In re claim 21, **Fisher** discloses that the CMOS structure is a p-channel CMOS structure, the shallow region comprising an n-type dopant (col. 4, line 45 to col. 5, line 54).

In re claim 22, **Fisher** discloses a transistor structure formed according to the method of claim 13 (FIG. 9).

Response to Applicant's Amendment and Arguments

Applicant's arguments with respect to claims 1-22 have been considered but are moot in view of the new ground(s) of rejection.

Applicants contend that Claim 1 requires, among other steps, the step of implanting a first dopant that has a lower concentration than that of the associated LDD region into the lightly doped drain (LDD) region to a depth less than a LDD junction depth. Applicants stated that no such step is taught or suggested by Mandelman either alone in the combination as claimed.

In response to Applicants' contention that Mandelman does not teach or suggest the step of implanting a first dopant that has a lower concentration than that of the associated LDD region into the lightly doped drain (LDD) region to a depth less than a LDD junction depth.

Examiner respectfully submits that Applicants' argument is moot since Applicant's amendment necessitated the new ground(s) of rejection presented in this

Office action. The newly discovered reference to Fisher (U.S. Patent 6,391,733) applied under 35 U.S.C. 102(b) rejection teaches the Applicants' claimed invention (Applicants are directed to page 2, 2nd paragraph to page 3, 1st paragraph presented in this Office Action) where Fisher discloses implanting a first dopant **100** has a lower dopant concentration (10^{12}-10^{15} atoms/cm^2) than that of the associated **120** LDD region **46,48** (1x 10^{12}- 1x10^{16} atoms/cm^2) into the lightly doped drain (LDD) region **46, 48** to a depth less than a LDD junction depth (col. 4, line 45 to col. 5, line 34 and FIG. 7); and implanting a second dopant **130** into the substrate **12** beyond the LDD junction depth to form a source/drain region **54,64,** the implantation of the second dopant overpowering (5x10^{14}-1x10^{16}) atoms/cm^2 a substantial portion of the first dopant to define a floating region **52, 62** of the first dopant within the LDD region 46, 48 (col. 5, lines 43-54 and FIG. 9).

For this reason, Examiner holds the rejection proper.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the

advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D. Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:30 AM - 5:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K.N.
July 22nd, 2005

W. DAVID COLEMAN
PRIMARY EXAMINER